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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,381	07/22/2006	Yoshiyuki Hojo	40404.44/ko	1240

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
08/28/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/597,381	HOJO, YOSHIYUKI	
	Examiner	Art Unit	
	DHARTI H. PATEL	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,6,8 and 9* is/are rejected.

7)☒ Claim(s) *7,10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/22/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5-6 and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitsuda, Patent No. 5,973,551.

With respect to claim 5, Mitsuda discloses an overcurrent detection circuit [Fig. 2] which detects an overcurrent when the overcurrent flows to an output transistor [Fig. 2; transistor Q1] including an input terminal [Fig. 2; drain of transistor Q1] to which a supply voltage [Fig. 2; Vcc] is input, a control terminal to which a control voltage is input [Fig. 2; gate terminal of transistor Q1, which is controlled by control circuit 1], and an output terminal from which an output current is output [Fig. 2; output terminal of Q1], the overcurrent detection circuit comprising: a monitor transistor [Fig. 2; transistor Q4] including a control terminal and an output terminal which are connected to the control terminal and the output terminal respectively of the output transistor [Fig. 2; gate terminals of transistors Q1 and Q4, and drain terminals of transistors Q1 and Q4 are connected]; an output current detection transistor [Fig. 2; transistor Q3] including an input terminal to which a supply voltage is input [Fig. 2; Vcc], a control terminal to which a detection bias voltage is input, and an output terminal which is connected to an input terminal of the monitor transistor [Fig. 2; source terminal of transistor Q3 is connected to

the drain terminal of transistor Q4]; a constant current source [Fig. 2; current source 3] that generates a reference current; a reference transistor [Fig. 2; transistor Q2] including an input terminal to which a supply voltage is input, a control terminal to which the detection bias voltage is input, and an output terminal from which the reference current flows to the constant current source; and a comparison circuit [Fig. 2; comparator 2] that detects an overcurrent when the overcurrent flows to the output transistor [Fig. 2; Q1] by comparing the voltage of the output terminal of the output current detection transistor [Fig. 2; Q3] and the voltage of the output terminal of the reference transistor [Fig. 2; Q2], and outputs an overcurrent detection signal [Fig. 2; signal coming out from control circuit 1 and going to the gate terminal of the output transistor Q1; col. 4 lines 30 – col. 5 lines 62].

With respect to claim 6, Mitsuda discloses that the output transistor [Fig. 2; Q1], the monitor transistor [Fig. 2; Q4], the output current detection transistor [Fig. 2; Q3], and the reference transistor [Fig. 2; Q2] are P-type MOS transistors [col. 7 lines 27-31].

With respect to claims 8-9, Mitsuda discloses the output transistor [Fig. 2; Q1] is provided between a supply voltage [Fig. 2; Vcc] and an output terminal that outputs a predetermined DC voltage, and the regulator further includes a control circuit [Fig. 2; control circuit 1] that controls the output transistor to maintain the predetermined DC voltage by inputting the voltage of the output terminal as feedback and that turns off the output transistor when the overcurrent detection signal of the overcurrent detection circuit [Fig. 2; output signal from the comparator 2] is input to the control circuit [col. 5 lines 41-63].

Allowable Subject Matter

Claims 7 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 7: The prior art does not disclose that the comparison circuit comprises a diode-connected first comparison transistor that is interposed between the constant current source and the reference transistor; a second constant current source that generates a current that is a predetermined multiple of the reference current generated by the constant current source; and a second comparison transistor that is interposed between the second constant current source and the output current detection transistor, a control terminal of the second comparison transistor being connected to a control terminal of the first comparison transistor. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DHARTI H. PATEL whose telephone number is (571)272-8659. The examiner can normally be reached on 7:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

/Dharti H Patel/
Examiner, Art Unit 2836
08/25/2008